



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/658,372	09/10/2003	Tsutomu Shoki	Q77434	3326
23373	7590	05/02/2006	EXAMINER	
SUGHRUE MION, PLLC 2100 PENNSYLVANIA AVENUE, N.W. SUITE 800 WASHINGTON, DC 20037			RUGGLES, JOHN S	
			ART UNIT	PAPER NUMBER
			1756	

DATE MAILED: 05/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/658,372	Applicant(s) SHOKI, TSUTOMU	
	Examiner John Ruggles	Art Unit 1756	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 10 February 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-12 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-12 is/are rejected.
- 7) ☒ Claim(s) 1-7 and 11-12 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 28 June 2004 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION***Election/Restrictions***

Applicant's election with traverse of Group I claims 1-5 and 8-10 in the reply filed on 2/10/06 is acknowledged. The traversal is on the ground(s) that the claims in Groups II and III are neither independent nor distinct from the claims in Group I. This is found persuasive and the previous restriction requirement is now withdrawn.

Therefore, claims 1-12 are pending and under consideration.

Drawings

Figure 4 should be designated by a legend such as --Prior Art--, because only that which is old is illustrated (since this drawing represents a “comparative example” to that of Figure 2, except without any heat treatment, while the instantly claimed and described invention requires heat treatment for the multilayer reflective mask blank). See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled “Replacement Sheet” in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

The title of the invention is not properly descriptive. A new title is required that is clearly indicative of the invention to which the claims must be directed.

Art Unit: 1756

The following title is suggested: --METHOD OF PRODUCING A REFLECTION [[TYPE]] MASK BLANK, METHOD OF PRODUCING A REFLECTION [[TYPE]] MASK, AND METHOD OF PRODUCING A SEMICONDUCTOR DEVICE--.

The abstract of the disclosure is objected to because: (1) it is written as a single sentence that is confusing; (2) in line 1, "reflection type mask blank" should be changed to --reflection [[type]] mask blank-- to more properly describe the enabled scope of the instant reflection mask blank (it is not clear what the word "type" was meant to include); (3) in lines 4-5 and 7-9, the statements about avoidance and suppression of interface mixing by heat treatment are not fully supported by the statements throughout the specification that the *change over lapsed time* in properties (e.g., compressive stress, etc.) of the multilayer reflector are suppressed by heat treatment (see e.g., page 4 line 25, page 5 line 20-22, comparison of Figure 4 (without heat treatment) and Figure 2 (with heat treatment), etc.); and (4) neither the claimed reflection mask nor the claimed method of producing a semiconductor device are included in this abstract.

Correction is required. See MPEP § 608.01(b).

35 U.S.C. 112, first paragraph, requires the specification to be written in "full, clear, concise, and exact terms." The specification is replete with terms, which are not clear, concise and exact. The specification should be revised carefully in order to comply with 35 U.S.C. 112, first paragraph. Examples of some unclear, inexact or verbose terms used in the specification are: (1) at page 2 lines 25 and 28, "the X-ray diffraction analysis" (in line 25) should be corrected to --[[the]] X-ray diffraction ~~analysis~~ analysis-- and "the level" (in line 28) should be changed to --[[the]] a level--; (2) at page 3 line 10, "causes the change in flatness of a substrate" should be amended (e.g., to --~~causes the~~ causing a change in flatness of a substrate--, etc.); (3) at

Art Unit: 1756

page 3 lines 21-22, "With respect to the above-mentioned object, the present inventor earnestly studied." is an incomplete sentence, which must be corrected; and (4) in the sentence bridging pages 4 and 5, "preferably not lower than 50°C and not higher than 135°C, not lower than 50°C and not higher than 100°C, more preferably not lower than 60°C and not higher than 100°C" should be changed to --preferably not lower than 50°C and not higher than 135°C, more preferably not lower than 50°C and not higher than 100°C, [[more]] and most preferably not lower than 60°C and not higher than 100°C--. Note that due to the number of errors, those listed here are merely examples of the corrections needed and do not represent an exhaustive list thereof.

Appropriate correction is required. An amendment filed making all appropriate corrections must be accompanied by a statement that the amendment contains no new matter and also by a brief description specifically pointing out which portion of the original specification provides support for each of these corrections.

Claim Objections

Claims 1-7 and 11-12 are objected to because of the following informalities: (1) in claim 1 lines 5 and 9, "in order to avoid mixing" (in line 5) should be changed to --in order to avoid progressive mixing-- and "the progress of the mixing" (in line 9) should be changed to --the progressive ~~of the~~ mixing-- and (2) in each of (a) claim 6 line 2 and (b) claim 11 line 2, it is suggested that "pattern on said absorber layer" be amended to --pattern [[on]] in said absorber layer--, since the reflection mask 101 illustrated in Figure 1D does **not** show any additional pattern **on** top of the absorber layer 14a, **but rather** the pattern has been formed **in** the absorber

Art Unit: 1756

layer 14a, itself. Claims 2-7 depend on claim 1, claim 7 depends on claim 6, and claim 12 depends on claim 11. Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In each of claims 1-12, the word "type" renders each of these claim(s) indefinite, because the claim(s) include(s) elements not actually disclosed (those encompassed by "type"), thereby rendering the scope of the claim(s) unascertainable. See MPEP § 2173.05(b) Part E "Type". Therefore, for the purpose of this Office action and in order to expedite the prosecution of this application, each of claims 1-12 have been interpreted with this word deleted --[[type]]--, at each occurrence.

In claim 4, "said resist" lacks proper antecedent basis and has therefore been interpreted to mean --[[said]] a resist--, for the purpose of this Office action.

In each of claims 6-8 and 11-12, "the step" lacks proper antecedent basis and has been interpreted to mean --[[the]] a step--, at each occurrence. Claims 9-12 depend on claim 8.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are

Art Unit: 1756

such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-2 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over either Mirkanimi (US 2001/0019803) or Mirkarimi et al. (US 6,319,635) in view of either Nguyen et al. (US 6,048,652), Levinson (Principles of Lithography, SPIE --The International Society for Optical Engineering), or Barbee, Jr. et al. (US 6,396,900).

Mirkanimi '19803 teaches reticles or masks, blanks therefore having multilayer reflective coatings or films for extreme ultraviolet (EUV) lithography, and methods of mitigating defects in such EUV multilayer reflective masks and blanks by depositing buffer and reflective coatings (of e.g., alternating layers of ion beam sputtered molybdenum (Mo)/silicon (Si), Mo/Be, Ru/Si, Si/Mo/Ru, etc., paragraph [0019]) and stress annealing (heat treating) such multilayer coatings at a compatible temperature in the range of about 100°C to 600°C for 0.001 hours (0.06 minutes) to 48 hours (e.g., annealing such multilayer coatings after deposition at a temperature of 300°C, 200°C, etc.), to achieve the desired stress and annealed surface roughness (claims, [0013], [0068]). The annealing or heating can be carried out during and/or after multilayer deposition ([0041], which is understood to mean that heat treatment is carried out before subsequent steps such as overcoating with an absorber and patterning using an overlying resist film to form an EUV multilayer reflective mask for lithography, instant claims 2 and 6). The multilayer buffer coating can be either the same material as the high reflecting multilayer film or a different material (abstract). Reflective coatings for EUV lithography are well known in the art ([0035]). The same ion beam sputtering tool can be used for depositing both the multilayer buffer coating and the overlying reflective coating ([0020]). The annealing or heating can be either slow or rapid, with the annealing temperature and time varying depending on the composition and

Art Unit: 1756

intended function of the multilayer coating (e.g., the multilayer buffer coating is permitted to have greater intermixing at layer interfaces and may be different in structure from the multilayer reflective film that is optimized for high reflectivity to EUV, etc., [0016], [0018], [0021], [0051]).

Mirkarimi et al. '635 teach similar reticles or masks, blanks therefore having multilayer reflective coatings or films for EUV lithography, and methods of mitigating defects in such EUV multilayer reflective masks and blanks by depositing buffer coatings under multilayer reflective films (of e.g., alternating layers of ion beam sputtered molybdenum (Mo)/silicon (Si), Mo/Be, Ru/Si, Si/Mo/Ru, etc., col. 3 lines 8-18) and stress annealing (heat treating) such multilayer coatings to achieve the desired stress and annealed surface roughness (claims). The annealing or heating can be carried out during and/or after multilayer deposition (col. 5 lines 14-15, which is understood to mean that heat treatment is carried out before subsequent steps such as overcoating with an absorber and patterning using an overlying resist film to form an EUV multilayer reflective mask for lithography, instant claims 2 and 6). The buffer coating can be either the same material as the reflective multilayer film or a different material (col. 3 lines 1-2).

Reflective coatings for EUV lithography are well known in the art (col. 4 lines 5-6). The same ion beam sputtering tool can be used for depositing both the multilayer buffer coating and the overlying reflective coating (col. 3 lines 19-26). The annealing or heating is carried out for the composition and intended function of the multilayer coating (e.g., the multilayer buffer coating is permitted to have greater intermixing at layer interfaces and may be different in structure from the multilayer reflective film that is optimized for high reflectivity to EUV, etc., col. 2 lines 49-51, col. 3 lines 3-7, col. 7 lines 24-26, 45-47, 52-55).

While specifically teaching heat treatment during and/or after multilayer deposition for optimization of the multilayer reflective film on the EUV mask or blank for less intermixing between layers (of e.g., Mo/Si, etc.) than is tolerated in a (multilayer) buffer coating (of e.g., Mo/Si, etc.) and other aspects of the instant claims, neither Mirkanimi '19803 nor Mirkarimi et al. '635 specifically teach that such heat treatment of the multilayer reflective film suppresses progressive mixing at the interface between reflective layers (of e.g., Mo/Si, etc.) after formation due to additional thermal factors (instant claim 1).

However, it is known in the art of making EUV multilayer reflective masks that Mo/Si alternating layers begin to intermix at about 150°C and this reduces reflectivity of the multilayer stack, so only low-temperature processes (e.g., for subsequent deposition and etching of an absorber layer through an overlying patterned resist film on the multilayer stack of a reflective mask blank to form a patterned EUV multilayer reflective mask, etc., instant claims 2 and 6) are used for fabricating such EUV multilayer reflective masks (as taught by Levinson (SPIE)). In fact, it is strongly preferred that any such processing occur at a temperature of less than about 150°C (including subsequent patterning of an absorber layer through an overlying patterned resist film on a multilayer reflective mask blank to form a patterned reflective mask, instant claims 2 and 6), in order to protect the integrity and quality of the Mo/Si reflective multilayer (as taught by Nguyen et al. col. 7 lines 3-7 and col. 8 lines 58-61). Furthermore, Barbee Jr. et al. teaches that Mo/Si multilayers cannot be exposed to temperatures above 120°C even for a short time (including subsequent etching procedures and thermal cycling to pattern masks having such reflective multilayers by patterning of an absorber layer through an overlying patterned resist film on a multilayer reflective mask blank to form a patterned reflective mask, instant claims 2

Art Unit: 1756

and 6), because the activation energy at the Mo/Si interface is so low that further diffusion and the growth of molybdenum silicide would be inevitable at this temperature, to avoid causing instability and degradation of the reflectance and multilayer period thickness needed for reflecting the desired EUV or soft x-ray wavelength (col. 1 lines 51-61).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention in the method of producing an EUV multilayer reflective mask blank involving heat treatment of a multilayer (of e.g., Mo/Si reflective film, etc.) on a reflective mask blank and subsequent patterning into an EUV multilayer reflective mask (as taught by Mirkanimi '19803 or Mirkarimi et al. '635) to keep the temperatures for the heat treatment and other subsequent processes to less than about 150°C (as taught by Levinson (SPIE) or Nguyen et al.), or particularly less than 120°C (as taught by Barbee Jr. et al.), in order to avoid intermixing of Mo/Si that would cause reduction in reflectivity of the multilayer stack (as taught by Levinson (SPIE)), protect the integrity and quality of the Mo/Si reflective multilayer (as taught by Nguyen et al.), or particularly to suppress further or progressive diffusion and the growth of molybdenum silicide that would cause instability and degradation of the reflectance and multilayer period thickness needed for reflecting the desired EUV wavelength (as taught by Barbee Jr. et al.). Thus, heat treatment of the multilayer reflective film below about 150°C or particularly below 120°C would be expected to inherently suppress progressive mixing at the interface between the EUV reflective multilayers (of e.g., Mo/Si, etc.) on the mask blank and on the corresponding patterned EUV multilayer reflective mask after formation due to additional thermal factors when subsequent processing temperatures (e.g., for deposition and/or etching of an absorber layer for the mask, etc.) are kept below such a heat treatment temperature (instant claims 1-2 and 6).

Art Unit: 1756

Claims 3-4, 6-9, and 11-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over either Mirkanimi (US 2001/0019803) or Mirkarimi et al. (US 6,319,635) in view of either Nguyen et al. (US 6,048,652), Levinson (Principles of Lithography, SPIE --The International Society for Optical Engineering), or Barbee, Jr. et al. (US 6,396,900), and further in view of Kumada et al. (US 2003/0152845).

While teaching other aspects of the instant claims, neither Mirkanimi '19803, Mirkarimi et al. '635, Nguyen et al., Levinson (SPIE), nor Barbee, Jr. et al. specifically teach a chemically amplified resist for patterning the absorber layer on the multilayer reflection mask blank (instant claims 3 and 9) or heat treatment at a temperature that is between 50°C and the baking temperature of the resist (instant claims 4 and 8).

Kumada et al. teach a mask blank and a method of patterning to form a mask (title, abstract). The method includes irradiating or exposing a chemically amplified resist film 3 (instant claims 3 and 9) on the mask blank 6 shown in Figure 2A with either an active light or a radiant ray (e.g., electron beam exposure, etc.) as shown in Figure 2B, and then heat treatment of the exposed chemically amplified resist, causing an acid catalytic reaction [0051]. The resist is patterned by developing as shown in Figure 2C [0052] and an underlying light blocking or absorber layer on the mask blank is etched through the patterned chemically amplified resist as shown in Figure 2D, followed by removing residual resist to yield a patterned photomask or mask as shown in Figure 2E [0053]. This patterned mask has a high dimensional uniformity and semiconductor devices made from this mask also have a high dimensional uniformity for high quality semiconductor devices in high yields [0054]. In Example 1, a chemically amplified resist was baked and dried on a hot plate at 110°C for 10 minutes before exposure by an electron beam,

Art Unit: 1756

then the resist is post-exposure baked again under the same conditions (at 110°C for 10 minutes), followed by developing to pattern the resist with a good shape in exact accordance with design dimensions, and further processing to form a patterned mask in the same manner as described and shown in Figures 2D-2E [0069, 0071-0072].

It would have been obvious to one of ordinary skill in the art at the time of the invention in the method of producing an EUV multilayer reflective mask blank involving heat treatment of a multilayer (of e.g., Mo/Si reflective film, etc.) on a reflective mask blank and subsequent processes for patterning this mask blank into an EUV multilayer reflective mask at temperatures less than about 150°C or particularly less than 120°C (as taught by Mirkanimi '19803 or Mirkanimi et al. '635 and Levinson (SPIE), Nguyen et al., or Barbee Jr. et al.) to utilize a chemically amplified resist (instant claims 3 and 9) for patterning the absorber layer on the multilayer reflection mask blank that would only require baking or heat treatment of the resist at a relatively low temperature of 110°C (as taught by Kumada et al.) that is below that which would cause problems with the multilayer reflective film. This is because a chemically amplified resist for patterning the multilayer reflective mask would be expected to provide a high dimensional uniformity in the mask and in resulting semiconductor devices made from this mask, as well as providing a patterned mask having a good shape in exact accordance with design dimensions and leading to high quality semiconductor devices in high yields (as taught by Kumada et al., instant claims 6-7 and 11-12). At least the lower portion of the heat treatment range of about 100°C to 110°C taught by Mirkanimi '19803 reads on the instant heat treatment temperature of between 50°C and the baking temperature (e.g., 110°C, etc.) of the chemically amplified resist that is taught by Kumada et al. (instant claims 4 and 8).

Art Unit: 1756

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over either Mirkanimi (US 2001/0019803) or Mirkarimi et al. (US 6,319,635) in view of either Nguyen et al. (US 6,048,652), Levinson (Principles of Lithography, SPIE --The International Society for Optical Engineering), or Barbee, Jr. et al. (US 6,396,900), and further in view of Mangat et al. (US 6,596,465).

While teaching other aspects of the instant claim, neither Mirkanimi '19803, Mirkarimi et al. '635, Nguyen et al., Levinson (SPIE), nor Barbee, Jr. et al. specifically teach heat treatment of the multilayer reflection film in a heated liquid (instant claim 5).

Mangat et al. teach a method of manufacturing a semiconductor component that includes exposure to EUV with a reflective lithographic mask having a patterned absorber layer (title, abstract). Patterning of an absorber on a EUV reflective mask blank to form a patterned reflective mask includes pattern transfer into absorber layers (260, 250, and 240 as shown in Figure 2) and subsequent stripping of residual resist by a 10 minute immersion in a sulfuric acid and hydrogen peroxide solution heated to approximately 85°C to 90°C in order to avoid higher temperatures encountered during an alternative resist ashing process (that would typically be performed at greater than approximately 150°C and would cause damage to the multilayer reflective mask blank (col. 3 lines 46-49 and col. 4 lines 33-39).

It would have been obvious to one of ordinary skill in the art at the time of the invention in the method of producing an EUV multilayer reflective mask blank involving heat treatment of a multilayer (of e.g., Mo/Si reflective film, etc.) on a reflective mask blank and subsequent processes for patterning this mask blank into an EUV multilayer reflective mask at temperatures less than about 150°C or particularly less than 120°C (as taught by Mirkanimi '19803 or

Art Unit: 1756

Mirkarimi et al. '635 and Levinson (SPIE), Nguyen et al., or Barbee Jr. et al.) to carry out the heat treatment of the multilayer reflection film by immersion in a liquid heated to approximately 85°C to 90°C that can also be used for stripping of residual resist without a separate step therefore, in order to avoid higher temperatures that would cause damage to the multilayer reflective film while still being expected to inherently suppress progressive mixing at the interface between the EUV reflective multilayers (of e.g., Mo/Si, etc.) on the mask blank and even avoiding an additional step to shorten and/or simplify the method of producing the multilayer reflective mask blank and the resulting patterned multilayer reflective mask (instant claim 5).

Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over either Mirkanimi (US 2001/0019803) or Mirkarimi et al. (US 6,319,635) in view of either Nguyen et al. (US 6,048,652), Levinson (Principles of Lithography, SPIE --The International Society for Optical Engineering), or Barbee, Jr. et al. (US 6,396,900), further in view of Kumada et al. (US 2003/0152845), and further in view of Mangat et al. (US 6,596,465).

While teaching other aspects of the instant claim, neither Mirkanimi '19803, Mirkarimi et al. '635, Nguyen et al., Levinson (SPIE), nor Barbee, Jr. et al. specifically teach heat treatment of the multilayer reflection film in a heated liquid at a temperature that is between 50°C and the baking temperature of the resist (instant claim 10).

The teachings of Kumada et al. and Mangat et al. have been discussed above.

It would have been obvious to one of ordinary skill in the art at the time of the invention in the method of producing an EUV multilayer reflective mask blank involving heat treatment of a multilayer (of e.g., Mo/Si reflective film, etc.) on a reflective mask blank and subsequent

Art Unit: 1756

processes for patterning this mask blank into an EUV multilayer reflective mask at temperatures less than about 150°C or particularly less than 120°C (as taught by Mirkanimi '19803 or Mirkarimi et al. '635 and Levinson (SPIE), Nguyen et al., or Barbee Jr. et al.) to carry out the heat treatment of the multilayer reflection film by immersion in a liquid heated to approximately 85°C to 90°C and to use a chemically amplified resist baked at 110°C (as taught by Kumada et al. and Mangat et al.). A chemically amplified resist for patterning the multilayer reflective mask would be expected to provide a high dimensional uniformity in the mask and in resulting semiconductor devices made from this mask, as well as providing a patterned mask having a good shape in exact accordance with design dimensions and leading to high quality semiconductor devices in high yields (as taught by Kumada et al.). The use of a chemically amplified resist would also avoid a higher baking temperature that would cause damage to the multilayer reflective film, while still allowing sufficient heat treatment to inherently suppress progressive mixing at the interface between the EUV reflective multilayers (of e.g., Mo/Si, etc.) on the mask blank. At least the lower portion of the heat treatment range of about 100°C to 110°C taught by Mirkanimi '19803 as well as the liquid heat treatment of 85°C to 90°C taught by Mangat et al. reads on the instant heat treatment temperature of between 50°C and the baking temperature of the chemically amplified resist (e.g., 110°C, etc.) that is taught by Kumada et al. (instant claim 10).

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined

Art Unit: 1756

application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1-2 and 6 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 23 of U.S. Patent No. 5,958,627 (Shoki '627) in view of either Mirkanimi (US 2001/0019803) or Mirkarimi et al. (US 6,319,635), and further in view of either Nguyen et al. (US 6,048,652), Levinson (Principles of Lithography, SPIE --The International Society for Optical Engineering), or Barbee, Jr. et al. (US 6,396,900). The conflicting claim of the Shoki '627 patent is not identical to the instant claims, at least because the Shoki '627 patent claim recites a method of producing an x-ray mask blank having an absorber film on an x-ray transparent film on a substrate that includes stress annealing or heat treatment, whereas the instant claims recite a method of producing a multilayer reflection mask blank having an absorber layer on a multilayer reflection film on a substrate that involves heat treatment to avoid progressive mixing at an interface between layers due to thermal factors in the reflection film. The Shoki '627 patent claim also does not specifically recite other instantly claimed limitations taught by the other references that are discussed above.

However, it would still have been obvious to one of ordinary skill in the art at the time of the invention that an x-ray mask and an EUV multilayer reflective mask are both usable for lithographic exposure of resists at overlapping or similar wavelengths. Other differences between the Shoki '627 patent claim and the instant claims are met by Mirkanimi '19803) or Mirkarimi et al. '635) and either Nguyen et al. (US 6,048,652), Levinson (SPIE), or Barbee, Jr. et al., each of which have been discussed above. Heat treatment of the multilayer reflective film below about 150°C or particularly below 120°C would be expected to inherently suppress progressive mixing at the interface between the EUV reflective multilayers (of e.g., Mo/Si, etc.) on the mask blank and on the corresponding patterned EUV multilayer reflective mask after formation due to additional thermal factors when subsequent processing temperatures (e.g., for deposition and/or etching of an absorber layer for the mask, etc.) are kept below such a heat treatment temperature (instant claims 1-2 and 6).

Claims 1-2 and 6-7 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-2 and 8-9 of copending Application No. 10/644,964 (Shoki '964) in view of either Mirkanimi (US 2001/0019803) or Mirkarimi et al. (US 6,319,635), and further in view of either Nguyen et al. (US 6,048,652), Levinson (Principles of Lithography, SPIE --The International Society for Optical Engineering), or Barbee, Jr. et al. (US 6,396,900). The conflicting claims of the Shoki '964 application are not identical to the instant claims, at least because the Shoki '964 application claims recite a method of manufacturing a multilayer reflection mask blank having a stress correction film along with an absorber film on a multilayer reflection film on a substrate that includes stress-affecting heat treatment, a method of manufacturing a reflection mask from the multilayer reflection mask

Art Unit: 1756

blank, and a method of manufacturing a semiconductor device by lithography using the multilayer reflection mask. The instant claims recite a method of producing a multilayer reflection mask blank having an absorber layer on a multilayer reflection film on a substrate without a stress correction film that involves heat treatment to avoid progressive mixing at an interface between layers due to thermal factors in the reflection film, a method of producing a multilayer reflection mask from the multilayer reflection mask blank, and a method of manufacturing a semiconductor device by lithography using the multilayer reflection mask. The Shoki '964 application claims also do not specifically recite other instantly claimed limitations that are taught by the other references, which have been discussed above.

However, it would still have been obvious to one of ordinary skill in the art at the time of the invention that the heat treatment of the multilayer reflective mask blank having a stress correction film in the Shoki '964 application claims could have alternatively been performed on a multilayer reflective mask blank without a stress correction film in the manner taught by either Mirkanimi '19803) or Mirkarimi et al. '635) and either Nguyen et al. (US 6,048,652), Levinson (SPIE), or Barbee, Jr. et al., each of which have been discussed above. Heat treatment of the multilayer reflective film below about 150°C or particularly below 120°C would be expected to inherently suppress progressive mixing at the interface between EUV reflective multilayers (of e.g., Mo/Si, etc.) on the mask blank and on the corresponding patterned EUV multilayer reflective mask after formation due to additional thermal factors when subsequent processing temperatures (e.g., for deposition and/or etching of an absorber layer for the mask, etc.) are kept below such a heat treatment temperature (instant claims 1-2 and 6). The method of producing a semiconductor device by lithography using such a heat treated multilayer reflective mask (instant

Art Unit: 1756

claim 7) would also have been obvious from Shoki '964 application claim 9 in combination with either Mirkanimi '19803) or Mirkarimi et al. '635) and either Nguyen et al. (US 6,048,652), Levinson (SPIE), or Barbee, Jr. et al. for the above stated reasons.

This is a provisional obviousness-type double patenting rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John Ruggles whose telephone number is 571-272-1390. The examiner can normally be reached on Monday-Thursday and alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Huff can be reached on 571-272-1385. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John Ruggles
Examiner
Art Unit 1756



**S. ROSASCO
PRIMARY EXAMINER
GROUP 1500**